IN THE CLAIMS

For the convenience of the Examiner, all pending claims of the present Application are shown below whether or not an amendment has been made.

Please amend the claims as follows.

1. **(Currently amended)** A method for switching between multiple clock signals in a digital circuit, comprising:

providing to a clock selector at least three distinct clock signals for a circuit;

generating on a master clock output of the clock selector a first master clock signal for the circuit based on a first one of the distinct clock signals;

asynchronously blocking the master clock output **in response to an inhibit signal**;

generating on the master clock output a second master clock signal for the circuit based on a second one of the distinct clock signals; and

synchronously unblocking the master clock output.

2. **(Previously presented)** The method of Claim 1, further comprising synchronously blocking the master clock output prior to asynchronously blocking the master clock output.

3. **(Previously presented)** The method of Claim 2, synchronously blocking the master clock output comprising blocking the master clock output in response to a first inhibit signal and a clock edge of the first distinct clock signal and asynchronously blocking the master clock output comprising blocking the master clock output in response to a second inhibit signal.

4. **(Previously presented)** The method of Claim 1, further comprising asynchronously unblocking the master clock output prior to synchronously unblocking the master clock output.

5. **(Previously presented)** The method of Claim 4, asynchronously unblocking the master clock output comprising unblocking the master clock output in response to a first non-inhibit signal and synchronously unblocking the master clock output comprising unblocking the master signal in response to a second non-inhibit signal and a clock edge of the second distinct clock signal.

6. **(Canceled)**

7. **(Previously presented)** The method of Claim 1, synchronously unblocking the master clock output comprising unblocking the master clock output in response to a non-irhibit signal and a clock edge of the second distinct clock signal.

8. **(Original)** A system for switching between multiple clock signals in a digital circuit, comprising:

a state machine operable to generate an inhibit signal and a non-inhibit signal;

a clock selector coupled to the state machine, the clock selector operable to receive at least three distinct clock signals and to select one of the distinct clock signals as a master clock signal for the circuit;

a synchronizer coupled to the state machine and the clock selector;

a synchronous gate coupled to the clock selector and the synchronizer, the synchronous gate and the synchronizer operable to synchronously unblock the master clock signal from the clock selector based on the non-inhibit signal from the state machine and to synchronously block the master clock signal from the clock selector based on the inhibit signal from the state machine; and

an asynchronous gate coupled to the state machine and the synchronous gate, the asynchronous gate operable to asynchronously unblock the master clock signal from the synchronous gate based on the non-inhibit signal from the state machine and to asynchronously block the master clock signal from the synchronous gate based on the inhibit signal from the state machine.

9. **(Original)** The system of Claim 8, the synchronizer further operable to receive the inhibit signal from the state machine, detect a clock edge for a first one of the distinct clock signals, and provide the inhibit signal to the synchronous gate in response to the clock edge for the first distinct clock signal.

10. **(Original)** The system of Claim 9, the synchronous gate further operable to block the master clock signal in response to the inhibit signal from the synchronizer.

11. **(Original)** The system of Claim 8, the synchronizer further operable to receive the non-inhibit signal from the state machine, to detect a clock edge for a second one of the distinct clock signals and to provide the non-inhibit signal to the synchronous gate in response to the clock edge for the second distinct clock signal.

12. **(Original)** The system of Claim 11, the synchronous gate further operable to unblock the master clock signal in response to the non-inhibit signal from the synchronizer.

13. **(Original)** The system of Claim 8, wherein the state machine is implemented in an application-specific integrated circuit.

14. **(Currently amended)** A system for switching between multiple clock signals in a digital circuit, comprising:

a computer-readable medium; and

logic stored on the computer-readable medium, the logic operable to generate on a master clock output a first master clock signal for the circuit based on a first one of at least three distinct clock signals, **to generate an inhibit signal,** to asynchronously block the master clock output **in response to the inhibit signal**, to generate on the master clock output a second master clock signal for the circuit based on a second one of the distinct clock signals, and to synchronously unblock the master clock output.

15. **(Canceled)**

16. **(Previously presented)** The system of Claim 14, the logic further operable to generate a non-inhibit signal and to synchronously unblock the master clock output in response to the non-inhibit signal.

17. **(Previously presented)** The system of Claim 14, the logic further operable to asynchronously unblock the master clock output prior to synchronously unblocking the master clock output.

18. **(Previously presented)** The system of Claim 14, the logic further operable to block the master clock output in response to a clock edge for the first distinct clock signal.

19. **(Previously presented)** The system of Claim 14, the logic further operable to unblock the master clock output in response to a clock edge for the second distinct clock signal.

20. **(Previously presented)** A method for switching between multiple clock signals in a digital circuit, comprising:

providing to a clock selector at least three distinct clock signals for the circuit;

generating on a master clock output of the clock selector a first master clock signal for the circuit based on a first one of the distinct clock signals;

generating an inhibit signal;

blocking the master clock output in response to the inhibit signal;

generating with the clock selector a second master clock signal for the circuit based on a second one of the distinct clock signals;

generating a non-inhibit signal;

detecting a clock edge for the second distinct clock signal; and

unblocking the master clock output in response to the non-inhibit signal and the clock edge for the second distinct clock signal.

21. **(Previously presented)** The method of Claim 20, further comprising:

detecting a clock edge for the first distinct clock signal; and

blocking the master clock output in response to the inhibit signal by blocking the master clock signal in response to the inhibit signal and the clock edge for the first distinct clock signal.

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. **(Currently amended)** A system for switching between multiple clock signals in a digital circuit, comprising:

means for providing to a clock selector at least two distinct clock signals for a circuit;

means for generating on a master clock output of the clock selector a first master clock signal for the circuit based on a first one of the distinct clock signals;

means for asynchronously blocking the master clock output **in response to an inhibit signal**;

means for generating on the master clock output a second master clock signal for the circuit based on a second one of the distinct clock signals; and

means for synchronously unblocking the master clock output.

26. **(Previously presented)** A system for switching between multiple clock signals in a digital circuit, comprising:

a state machine operable to generate a first inhibit signal and a second inhibit signal and a first non-inhibit signal and a second non-inhibit signal;

a clock selector coupled to the state machine, the clock selector operable to receive a plurality of distinct clock signals and to select one of the distinct clock signals as a master clock signal for the circuit;

a synchronizer coupled to the state machine and the clock selector;

a synchronous gate coupled to the clock selector and the synchronizer, the synchronous gate and the synchronizer operable to synchronously unblock the master clock signal received from the clock selector based on the first non-inhibit signal from the state machine and to synchronously block the master clock signal received from the clock selector based on the first inhibit signal from the state machine; and

an asynchronous gate coupled to the state machine and the synchronous gate, the asynchronous gate operable to asynchronously unblock the master clock signal received from the synchronous gate based on the second non-inhibit signal from the state machine and to asynchronously block the master clock signal received from the synchronous gate based on the second inhibit signal from the state machine.

27. **(Previously presented)** The system of Claim 26, the synchronizer further operable to receive the first inhibit signal from the state machine, detect a clock edge for a first one of the distinct clock signals, and provide the first inhibit signal to the synchronous gate in response to the clock edge for the first distinct clock signal.

28. **(Previously presented)** The system of Claim 27, the synchronous gate further operable to block the master clock signal in response to the first inhibit signal from the synchronizer.

29. **(Previously presented)** The system of Claim 26, the synchronizer further operable to receive the first non-inhibit signal from the state machine, to detect a clock edge for a second one of the distinct clock signals and to provide the first non-inhibit signal to the synchronous gate in response to the clock edge for the second distinct clock signal.

30. **(Previously presented)** The system of Claim 29, the synchronous gate further operable to unblock the master clock signal in response to the first non-inhibit signal from the synchronizer.

31. **(Previously presented)** The system of Claim 26, wherein the state machine is implemented in an application-specific integrated circuit.